ABSTRACT OF THE DISCLOSURE

An arbiter circuit minimizes the occurrence of malfunctions and permits easy adjustment. The arbiter circuit includes a data transfer request signal holding device for accepting a plurality of data transfer request signals and holding the data transfer request signals in response to predetermined timing signals, a prioritizing device for determining only a signal with the highest priority at a certain point as a valid signal and the signals with lower priorities as invalid signals in order to assign priorities to output signals from the data transfer request signal holding device, and a delaying device for generating data transfer execution signals from the output signals of the prioritizing device. This arrangement restrains the occurrence of errors in assigning priorities to data transfer request signals and permits easy priority timing setting, thus allowing easy adjustment of a circuit to be achieved.